WHAT IS CLAIMED IS:

1. A timing adjustment device for adjusting the timing at a bus interface and preventing any read/write error due to timing deviation, the adjustment device comprising:

a cycle protocol device for generating a special read/write cycle signal that links up with devices having connection with the bus interface;

a phase lock loop device coupled to the bus interface for receiving an internal clocking signal, increasing/decreasing the amount of phase shift in the internal clocking signal to become a clocking signal for the bus interface to drive a special read/write test sample to a bus and trigger the reception of data on the bus;

a special pattern device coupled to the cycle protocol device, wherein the special pattern device generates the special read/write test samples according to the special read/write cycle signal to provide read/write tests of the bus interface and check the bus interface for the correctness of data read/write operation; and

an add/subtract device coupled to the phase lock loop device for setting the amount of phase shift in the phase lock loop device.

2. The timing adjustment device of claim 1, wherein the phase lock loop device further receives a signal N for setting the phase shift resolution of the amount of phase shift in the phase lock loop device.

3. A timing adjustment device for a system bus interface, wherein the system bus interface is coupled to a system bus and the system bus is coupled to a central processing unit (CPU), the timing adjustment device comprising:

a cycle protocol device for outputting a timing adjusting signal to adjust the system bus interface;

a special pattern device coupled to the cycle protocol device and the system bus interface for sending a special sample format signal to the system bus interface during the special timing cycle in response of the timing adjusting signal;

an add/subtract device for outputting a phase signal according to an add/subtract signal;

a phase lock loop device coupled to the add/subtract device and the system bus interface for receiving the phase signal and an internal clocking signal, wherein the phase lock loop device shifts the internal clocking signal according to the phase signal, and outputs a phase-shifted clocking signal; and

a core logic device coupled to the central processing unit and the add/subtract device for sending a central processing unit reset signal to the central processing unit and asserting the add/subtract control signal when adjusting the system bus interface;

wherein the system bus interface adjusts and drives the special sample format signal to the system bus interface according to the phase-shifted clocking signal.

4. The timing adjustment device of claim 3, wherein the core logic device also asserts the central processing unit reset signal and add/subtract control signal repeatedly a number of times to obtain the optimum phase signal for operating the system bus interface.

5. The timing adjustment device of claim 3, wherein the system bus interface further comprises:

a latching device coupled to the special pattern device and the phase lock loop device for registering the special sample format signal and using the phase-shifted

clocking signal as a timing signal to drive the latching device so that the latching device outputs an adjusted special sample format signal; and

a buffer coupled to the latching device for receiving the adjusted special sample format signal, boosting the current of the adjusted special sample format signal and sending the adjusted special sample format signal to the central processing unit.

6. The timing adjustment device of claim 5, wherein the central processing unit interface further comprises:

a drive-boosting controller coupled to the buffer for outputting a drive-boosting signal and controlling the driving capability of the buffer.

7. The timing adjustment device of claim 3, wherein the phase lock loop device further receives a signal N for determining the phase value in each shifting of the internal clocking signal.

8. A control chipset coupled to a central processing unit via a system bus, comprising:

a system bus interface coupled to the system bus for latching and buffering the signals between the control chipset and the central processing unit; and

a timing adjustment device coupled to the system bus interface for controlling the system bus interface, adjusting the timing of signal between the control chipset and the system bus, the timing adjustment device further comprising:

a cycle protocol device for outputting a timing adjusting signal to adjust the system bus interface;

a special pattern device coupled to the cycle protocol device and the system bus interface for sending a special sample format signal to the system bus interface during the special timing cycle in response of the timing adjusting signal;

an add/subtract device for outputting a phase signal according to an add/subtract signal;

a phase lock loop device coupled to the add/subtract device and the system bus interface for receiving the phase signal and an internal clocking signal, wherein the phase lock loop device shifts the internal clocking signal according to the phase signal, and outputs a phase-shifted clocking signal;and

a core logic device coupled to the central processing unit and the add/subtract device for sending a central processing unit reset signal to the central processing unit and asserting the add/subtract control signal when adjusting the system bus interface;

wherein the system bus interface adjusts and drives the special sample format signal to the system bus according to the phase-shifted clocking signal.

9. The control chipset of claim 8, wherein the core logic device also asserts the central processing unit reset signal and add/subtract control signal repeatedly a number of times to obtain the optimum phase signal for operating the system bus interface.

10. The control chipset of claim 8, wherein the system bus interface further comprises:

a latching device coupled to the special pattern device and the phase lock loop device for registering the special sample format signal and using the phase-shifted clocking signal as a timing signal to drive the latching device so that the latching device outputs an adjusted special sample format signal; and

a buffer coupled to the latching device for receiving the adjusted special sample format signal, boosting the current of the adjusted special sample format signal and sending the adjusted special sample format signal to the central processing unit.

11. The control chipset of claim 10, wherein the system bus interface further comprises:

a drive-boosting controller coupled to the buffer for outputting a drive-boosting signal and controlling the driving capability of the buffer.

12. A method of adjusting the timing of a system bus interface, wherein the system bus interface is coupled to a system bus and the system bus is coupled to a central processing unit, the method comprising the steps of:

sending a central processing unit reset signal to the central processing unit;

sending an add/subtract signal;

phase-shifting an internal clocking signal according to the add/subtract signal and outputting a phase-shifted clocking signal;

sending a first special sample format signal to the system bus interface according to a special timing cycle;

adjusting a feedback signal from the system bus to produce a second special sample format signal according to the phase-shifted clocking signal;

receiving the second special sample format signal from the system bus interface according to the special timing cycle;

comparing the first special sample format signal with the second special sample format signal to determine if there is any error or not; and

if not, sending out the central processing unit reset signal and the add/subtract control signal several times to obtain the optimum phase adjusting signal for operating the system bus interface.

13. A timing adjustment device for a system bus interface, wherein the system bus interface is coupled to a system bus and the system bus is coupled to a central processing unit (CPU), the timing adjustment device comprising:

a cycle protocol device for outputting a timing adjusting signal to adjust the system bus interface;

a special pattern device coupled to the cycle protocol device and the system bus interface for receiving a special sample format signal from the system bus interface during the special timing cycle in response of the timing adjusting signal;

an add/subtract device for outputting a phase signal according to an add/subtract signal;

a phase lock loop device coupled to the add/subtract device and the system bus interface for receiving the phase signal and an internal clocking signal, wherein the phase lock loop device shifts the internal clocking signal according to the phase signal and outputs a phase-shifted clocking signal; and

a core logic device coupled to the central processing unit and the add/subtract device for sending a central processing unit reset signal to the central processing unit and asserting the add/subtract control signal when adjusting the system bus interface;

wherein the system bus interface adjusts and drives a result signal of the system bus to become the special sample format signal according to the phase-shifted clocking signal.

14. The timing adjustment device of claim 13, wherein the core logic device also asserts the central processing unit reset signal and add/subtract control signal repeatedly a

number of times to obtain the optimum phase signal for operating the system bus interface.

15. The timing adjustment device of claim 13, wherein the system bus interface further comprises:

a buffer for receiving the result signal from the central processing unit, boosting the current of the result signal and outputting the result signal; and

a latching device coupled to the special pattern device, the phase lock loop device and the buffer for receiving and holding the result signal and using the phase-shifted clocking signal as a timing signal to drive the latching device so that the latching device outputs the special sample format signal.

16. The timing adjustment device of claim 13, wherein the phase lock loop device further receives a signal N for determining the phase value in each shifting of the internal clocking signal.

17. A control chipset coupled to a central processing unit through a system bus, comprising:

a system bus interface coupled to the system bus for latching and buffering the signals between the control chipset and the central processing unit; and

a timing adjustment device coupled to the system bus interface for controlling the system bus interface, adjusting the timing of signal between the control chipset and the system bus, the timing adjustment device further comprising:

a cycle protocol device for outputting a timing adjusting signal to adjust the system bus interface;

a special pattern device coupled to the cycle protocol device and the system bus interface for receiving a special sample format signal from the system bus interface during the special timing cycle in response of the timing adjusting signal;

an add/subtract device for outputting a phase signal according to an add/subtract signal;

a phase lock loop device coupled to the add/subtract device and the system bus interface for receiving the phase signal and an internal clocking signal, wherein the phase lock loop device shifts the internal clocking signal according to the phase adjusting signal and outputs a phase-shifted clocking signal; and

a core logic device coupled to the central processing unit and the add/subtract device for sending a central processing unit reset signal to the central processing unit and asserting the add/subtract control signal when adjusting the system bus interface;

wherein the system bus interface adjusts and drives a result signal of the system bus to become the special sample format signal according to the phase-shifted clocking signal.

18. The control chipset of claim 17, wherein the core logic device also asserts the central processing unit reset signal and add/subtract control signal repeatedly a number of times to obtain the optimum phase signal for operating the system bus interface.

19. The control chipset of claim 17, wherein the system bus interface further comprises:

a buffer for receiving the result signal from the central processing unit, boosting the current of the result signal and outputting the boosted result signal; and

a latching device coupled to the special pattern device, the phase lock loop device and the buffer for receiving and holding the result signal and using the phase-shifted clocking signal as a timing signal to drive the latching device so that the latching device outputs the special sample format signal.

20. A timing adjustment device of a chip bus interface for adjusting the timing signal of the chip bus interface inside a first chip, wherein the chip bus interface is coupled to a bus and the bus is coupled to a second chip, and the second chip further includes a chip bus interface, the timing adjustment device comprising:

a cycle protocol device for generating a special timing cycle and outputting an expected timing signal when adjusting the timing of the chip bus interface inside the first chip;

a special pattern device coupled to the cycle protocol device and the chip bus interface of the first chip for receiving the expected timing signal and outputting a special sample format signal to the chip bus interface of the first chip during the special timing cycle;

an add/subtract device for increasing/decreasing a phase adjusting signal; and

a phase lock loop device coupled to the add/subtract device and the chip bus interface of the first chip for receiving the phase adjusting signal and an internal clocking signal, wherein the phase lock loop device shifts the internal clocking signal according to the phase adjusting signal and outputs a phase-shifted clocking signal, and the chip bus interface of the first chip adjusts and drives the special sample format signal to the bus according to the phase-shifted clocking signal;

wherein in the process of adjusting the chip bus interface of the first chip, the first chip increases/decreases and asserts the phase adjusting signal repeatedly several times so that the chip bus interface of the first chip adjusts and drives the special sample format signal to the bus repeatedly several times, and through the determination of the correctness of the special sample format signal received by the chip bus interface of the second chip, the optimum phase adjusting signal for operating the chip bus interface of the first chip is obtained.

21. The timing adjustment device of claim 20, wherein the chip bus interface of the first chip further comprises:

a latching device coupled to the special pattern device and the phase lock loop device for registering the special sample format signal and using the phase-shifted clocking signal as a timing signal to drive the latching device so that the latching device outputs an adjusted special sample format signal; and

a buffer coupled to the latching device for receiving the adjusted special sample format signal, boosting the current of the adjusted special sample format signal and sending the adjusted special sample format signal to the bus.

22. The timing adjustment device of claim 21, wherein the chip bus interface further comprises:

a drive-boosting controller coupled to the buffer for outputting a drive-boosting signal and controlling the driving capability of the buffer.

23. The timing adjustment device of claim 20, wherein the phase lock loop device further receives a signal N for determining the phase value in each shifting of the internal clocking signal.

24. A maim control chip of a control chipset coupled to a slave control chip via a bus, comprising:

a chip bus interface coupled to the bus for latching and buffering signals between the main control chip and the slave control chip; and

a timing adjustment device coupled to the chip bus interface for controlling the chip bus interface and adjusting the timing signal between the main control chip and the bus, and the timing adjustment device comprising:

a cycle protocol device for generating a special timing cycle and outputting an expected timing signal when adjusting the timing of the chip bus interface inside the main control chip;

a special pattern device coupled to the cycle protocol device and the chip bus interface of the main control chip for receiving the expected timing signal and outputting a special sample format signal to the chip bus interface of the main control chip during the special timing cycle;

an add/subtract device for increasing/decreasing a phase adjusting signal; and

a phase lock loop device coupled to the add/subtract device and the chip bus interface of the main control chip for receiving the phase adjusting signal and an internal clocking signal, wherein the phase lock loop device shifts the internal clocking signal according to the phase adjusting signal and outputs a phase-shifted clocking signal, and the chip bus interface of the main control chip adjusts and drives the special sample format signal to the bus according to the phase-shifted clocking signal;

wherein in the process of adjusting the chip bus interface of the main control chip, the main control chip increases/decreases and asserts the phase adjusting

signal repeatedly several times so that the chip bus interface of the first chip adjusts and drives the special sample format signal to the bus repeatedly several times, and through the determination of the correctness of the special sample format signal received by the slave control chip, the optimum phase adjusting signal for operating the chip bus interface of the main control chip is obtained.

25. The timing adjustment device of claim 24, wherein the chip bus interface of the main control chip further comprises:

a latching device coupled to the special pattern device and the phase lock loop device for registering the special sample format signal and using the phase-shifted clocking signal as a timing signal to drive the latching device so that the latching device outputs an adjusted special sample format signal; and

a buffer coupled to the latching device for receiving the adjusted special sample format signal, boosting the current of the adjusted special sample format signal and sending the adjusted special sample format signal to the bus.

26. The timing adjustment device of claim 25, wherein the chip bus interface further comprises:

a drive-boosting controller coupled to the buffer for outputting a drive-boosting signal and controlling the driving capability of the buffer.

27. The timing adjustment device of claim 24, wherein the main control chip is a north bridge control chip.

28. The timing adjustment device of claim 24, wherein the main control chip is a south bridge control chip.

29. A control chipset, comprising:

a first control chip coupled to a bus; comprising:

a chip bus interface coupled to the bus for latching and buffering the signals between the first control chip and the bus; and

a timing adjustment device coupled to the chip bus interface of the first control chip for controlling the chip bus interface of the first control chip and adjusting the timing of signals between the first control chip and the bus, and the timing adjustment device comprising:

a cycle protocol device for generating a special timing cycle and outputting an expected timing signal when adjusting the timing of the chip bus interface inside the first control chip;

a special pattern device coupled to the cycle protocol device and the chip bus interface of the first control chip for receiving the expected timing signal and outputting a special sample format signal to the chip bus interface of the first control chip during the special timing cycle;

an add/subtract device for increasing/decreasing a phase adjusting signal; and

a phase lock loop device coupled to the add/subtract device and the chip bus interface of the first control chip for receiving the phase adjusting signal and an internal clocking signal, wherein the phase lock loop device shifts the internal clocking signal according to the phase adjusting signal and outputs a phase-shifted clocking signal, and the chip bus interface of the first control chip adjusts and drives the special sample format signal to the bus according to the phase-shifted clocking signal;

a second control chip coupled to the bus, comprising:

a chip bus interface coupled to the bus for latching and buffering the signals between the second control chip and the bus; and

a special pattern device coupled to the chip bus interface of the second control chip;

wherein in the process of adjusting the chip bus interface of the first control chip, the first control chip increases/decreases and asserts the phase adjusting signal repeatedly several times so that the chip bus interface of the first control chip adjusts and drives the special sample format signal to the bus repeatedly several times, the chip bus interface of the second control chip receives the signals on the bus, and through the determination of the correctness of the special sample format signal received by the second control chip, the optimum phase adjusting signal for operating the chip bus interface of the first control chip is obtained.

30. A method of adjusting the timing of the chip bus interface of a first control chip, wherein the chip bus interface is coupled to a bus and the bus is coupled to a second control chip, and the second control chip further includes a chip bus interface, the timing adjustment method comprising the steps of:

sending a phase adjusting signal to shift an internal clocking signal and output a phase-shifted clocking signal;

according to a special timing cycle, sending a first special sample format signal to the chip bus interface of the first control chip;

according to the phase-shifted clocking signal, the chip bus interface of the first control chip adjusts and drives the first special sample format signal to the bus;

receiving the signals on the bus from the chip bus interface of the second control chip, the second control chip compares and determines if the first special sample format signal is correctly received or not; and

if correctly received, re-asserting the phase adjusting signal several times to obtain the optimum phase adjusting signal for operating the chip bus interface.

31. The timing method of claim 30, wherein the method further comprises the following steps:

according to the special timing cycle, the chip bus interface of the second control chip drives a second special sample format signal to the bus; and

according to the phase-shifted clocking signal, the chip bus interface of the first control chip adjusts and latches the signals on the bus, and the first control chip compares to determine if the second special sample format signal is correctly received.

32. A memory controller coupled to a memory bus that couples with a memory unit, the memory controller comprising:

a memory initialization device coupled to the memory bus for initializing the memory unit, wherein the memory unit may is able to operate normally only after the initialization;

a memory bus interface coupled to the memory bus for latching and buffering the signals between the memory controller and the memory unit; and

a timing adjustment device coupled to the memory bus interface for controlling the memory bus interface and adjusting the timing of signals between the memory controller and the memory bus, the timing adjustment device comprising:

a cycle protocol device for generating a special timing cycle and outputting an expected timing signal when adjusting the timing of the memory bus interface;

a special pattern device coupled to the cycle protocol device and the memory bus interface for receiving the expected timing signal, sending a first special sample format signal to the memory bus interface and receiving a second special sample format signal from the memory bus interface during the special timing cycle;

a first add/subtract device for increasing/decreasing a first phase adjusting signal;

a second add/subtract device for increasing/decreasing a second adjusting signal;

a first phase lock loop device coupled to the first add/subtract device and the memory bus interface for receiving the first phase adjusting signal and an internal clocking signal, wherein the first phase lock loop device shifts the internal clocking signal according to the first phase adjusting signal and outputs a first phase-shifted clocking signal, and the memory bus interface drives the first special sample format signal to the memory bus according to the first phase-shifted clocking signal; and

a second phase lock loop device coupled to the second add/subtract device and the memory bus interface for receiving the second phase adjusting signal and an internal clocking signal, wherein the second phase lock loop device shifts the internal clocking signal according to the second phase adjusting signal and outputs a second phase-shifted clocking signal, and the memory bus interface adjusts and drives the signals on the memory bus to become the second special sample format signal according to the second phase-shifted clocking signal;

wherein the first add/subtract device and the second add/subtract device increases/decreases and re-asserts the first phase adjusting signal and the second phase adjusting signal repeatedly a number of times and compares the received first special

sample format signal and the second special sample format signal to obtain the optimal phase adjusting signal for operating the memory bus interface.

33. The memory controller of claim 32, wherein the memory bus interface further includes:

a first latching device coupled to the special pattern device and the first phase lock loop device for registering the first special sample format signal and using the first phase-shifted clocking signal as a timing signal to drive the first latching device so that the first latching device outputs an adjusted first special sample format signal;

a first buffer coupled to the first latching device for receiving the adjusted first special sample format signal, boosting the current of the adjusted first special sample format signal and outputting the adjusted first special sample format signal to the memory unit; and

a drive-boosting controller coupled to the first buffer for outputting a drive-boosting signal to control the driving capability of the first buffer.

34. The memory controller of claim 33, wherein the memory bus interface further includes:

a second buffer for receiving, boosting and outputting signals on the memory bus; and

a second latching device coupled to the special pattern device, the second phase lock loop device and the second buffer for receiving and holding signals on the memory bus output from the second buffer and using the second phase-shifted clocking signal as a timing signal to drive the second latching device so that the second latching device outputs the adjusted second special sample format signal.

35. The memory controller of claim 32, wherein the first phase lock loop device and the second phase lock loop device further receives a signal N for determining the phase value in each shifting of the internal clocking signal.

36. A memory controller coupled to a memory bus that couples with a memory unit, the memory controller comprising:

a memory bus interface coupled to the memory bus for latching and buffering the signals between the memory controller and the memory unit; and

a timing adjustment device coupled to the memory bus interface for controlling the memory bus interface and adjusting the timing of signals between the memory controller and the memory bus, the timing adjustment device comprising:

a cycle protocol device for generating a special timing cycle and outputting an expected timing signal when adjusting the timing of the memory bus interface;

a special pattern device coupled to the cycle protocol device and the memory bus interface for receiving the expected timing signal, sending a special sample format signal to the memory bus interface during the special timing cycle;

an add/subtract device for increasing/decreasing a phase adjusting signal; and

a phase lock loop device coupled to the add/subtract device and the memory bus interface for receiving the phase adjusting signal and an internal clocking signal, wherein the phase lock loop device shifts the internal clocking signal according to the phase adjusting signal and outputs a phase-shifted clocking signal, and the memory bus interface drives the special sample format signal to the memory bus according to the phase-shifted clocking signal;

wherein the add/subtract device increases/decreases and re-asserts the phase adjusting signal repeatedly a number of times and checks the correctness of the special sample format signal received by the memory unit to obtain the optimal phase adjusting signal for operating the memory bus interface.

37. The memory controller of claim 36, wherein the memory bus interface further includes:

a latching device coupled to the special pattern device and the phase lock loop device for registering the special sample format signal and using the phase-shifted clocking signal as a timing signal to drive the latching device so that the latching device outputs an adjusted special sample format signal;

a buffer coupled to the latching device for receiving the adjusted special sample format signal, boosting the current of the adjusted special sample format signal and outputting the adjusted special sample format signal to the memory unit; and

a drive-boosting controller coupled to the buffer for outputting a drive-boosting signal to control the driving capability of the buffer.

38. The memory controller of claim 36, wherein the phase lock loop device further receives a signal N for determining the phase value in each shifting of the internal clocking signal.

39. A timing adjustment method for adjusting the memory bus interface of a memory controller, wherein the memory bus interface is coupled to a memory bus and the memory bus is coupled to a memory, the timing adjustment method comprising the steps of:

initializing the memory;

sending out a phase adjusting signal;

shifting an internal clocking signal according to the phase adjusting signal and sending out a phase-shifted clocking signal;

sending a first special sample format signal to the memory bus interface according to a special timing cycle;

according to the phase-shifted clocking signal, the memory bus interface drives the first special sample format signal to the memory bus;

according to the phase-shifted clocking signal, the memory bus interface receives the signals on the memory bus to produce a second special sample format signal;

receiving the second special sample format signal from the memory bus interface according to the special timing cycle;

comparing the first special sample format signal and the second special sample format signal; and

increasing/decreasing and re-asserting the phase adjusting signal repeatedly a number of times to obtain the optimal phase adjusting signal for operating the memory bus interface.